

ABSTRACT

Analog computational arrays for matrix-vector multiplication offer very large integration density and throughput as, for instance, needed for real-time signal processing in video. Despite the success of adaptive algorithms and architectures in reducing the effect of analog component mismatch and noise on system performance, the precision and repeatability of analog VLSI computation under process and environmental variations is inadequate for some applications. Digital implementation offers absolute precision limited only by wordlength, but at the cost of significantly larger silicon area and power dissipation compared with dedicated, fine-grain parallel analog implementation. The present invention comprises a hybrid analog and digital technology for fast and accurate computing of a product of a long vector (thousands of dimensions) with a large matrix (thousands of rows and columns). At the core of the externally digital architecture is a high-density, low-power analog array performing binary-binary partial matrix-vector multiplication. Digital multiplication of variable resolution is obtained with bit-serial inputs and bit-parallel storage of matrix elements, by combining quantized outputs from one or more rows of cells over time. Full digital resolution is maintained even with low-resolution analog-to-digital conversion, owing to random statistics in the analog summation of binary products. A random modulation scheme produces near-Bernoulli statistics even for highly correlated inputs. The approach has been validated by electronic prototypes achieving computational efficiency (number of computations per unit time using unit power) and integration density (number of computations per unit time on a unit chip area) each a factor of 100 to 10,000 higher than that of existing signal processors making the invention highly suitable for inexpensive micropower implementations of high-data-rate real-time signal processors.